AN10549

Design rules and schematics for LPC288x

Rev. 02 — 1 June 2007 Application note

Document information

Info	Content
Keywords	LPC2888, LPC2880, design rules, application schematic
Abstract	This application note provides design rules and application schematics for the various peripherals of the LPC288x.

Revision history

Rev	Date	Description
02	20070601	Added sections 15, 16, and 17
01	20070102	Initial version

Contact information

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1. Introduction

This application note provides design rules and schematics for most of the peripherals/blocks of the LPC288x. A complete listing of all the LPC288x modules covered in this application note is present in the “Contents” section.

For each module, the following sections are provided:

1. Overview
2. Application description
   a. Design rules
   b. Application schematic

2. 12 MHz oscillator

2.1 Overview

The LPC288x contains two oscillators: 12 MHz main oscillator and 32.768 kHz oscillator. The 12 MHz oscillator is mandatory and is used in combination with two PLLs and several clock dividers to generate the system frequencies.

2.2 Application description

2.2.1 Design rules

The LPC288x cannot function without the 12 MHz oscillator, so this part should always be connected. To guarantee correct operation use a crystal to drive the oscillator and do not use a ceramic resonator.

2.2.2 Application diagram

Fig 1 shows how the 12 MHz oscillator should be connected. Table 1 lists the crystal parameters together with external components.

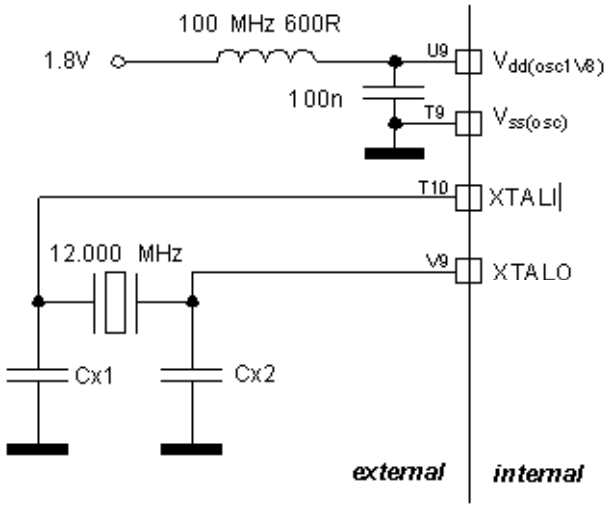


Fig 1. 12 MHz oscillator connection

Table 1. 12 MHz oscillator parameters and external components

Oscillation frequency f_c	Crystal load capacitance C_L	Max crystal series resistance $R_{S(max)}$	External load capacitors C_{x1}, C_{x2}
12 MHz	10 pF	160 Ω	18 pF
	20 pF	60 Ω	39 pF

3. 32.768 kHz oscillator

3.1 Overview

The LPC288x contains two oscillators: 12 MHz main oscillator and 32.768 kHz oscillator. The 32.768 kHz oscillator is not mandatory and is used to generate the frequency for the RTC.

3.2 Application description

3.2.1 Design rules

The LPC288x can function with or without the 32.768 kHz oscillator. While using this part use a crystal to drive the oscillator to guarantee correct operation and do not use a ceramic resonator.

3.3 Application diagram

Fig 2 shows how the 32.768 kHz should be connected when used and when not used. If the part is not used then leave the supply on and tie the input (pin V7) to ground. The supply should be left on because the internal PLLs are also supplied from this part.

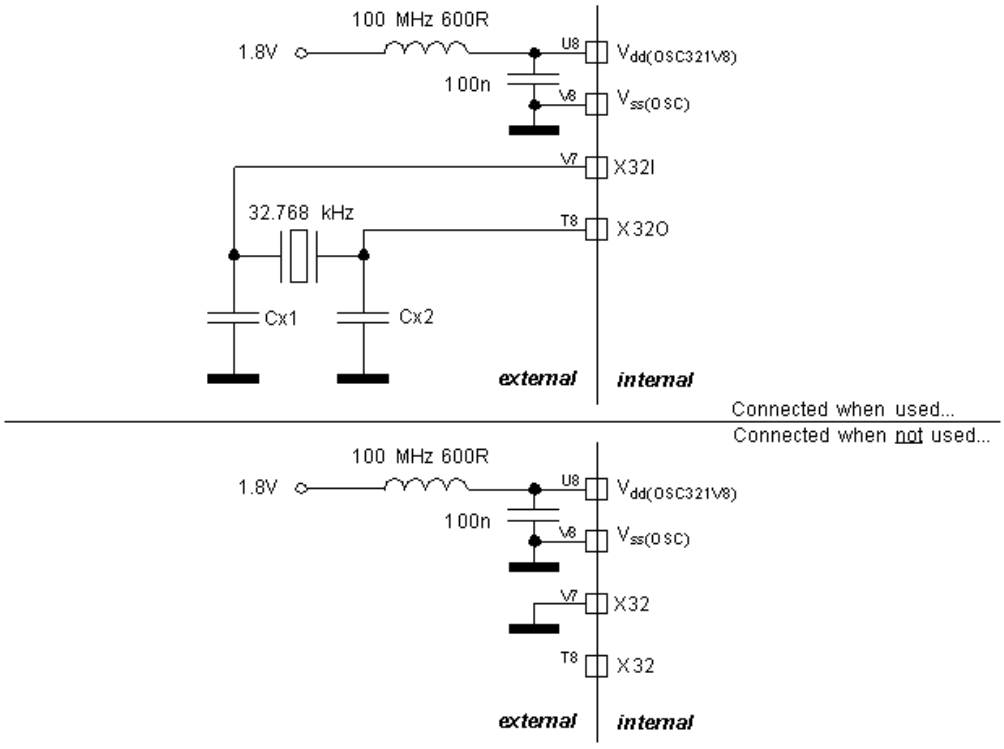


Fig 2. 32.768 kHz oscillator connection

Table 2 lists the crystal parameters together with external components.

Table 2. 32.768 kHz oscillator parameters and external components

Oscillation frequency f_c	Crystal load capacitance C_L	Max crystal series resistance $R_{S(max)}$	External load capacitors C_{x1}, C_{x2}
32.768 kHz	11 pF	100 Ω	18 pF
	13 pF	100 Ω	22 pF
	15 pF	100 Ω	27 pF

4. 10-bit ADC

4.1 Overview

1. 10 bit successive approximation analog to digital converter.
2. Input multiplexing among 5 pins.
3. Power down mode.
4. Measurement range 0 V to 3 V.
5. 10 bit conversion time ≥ 2.44 µs.
6. Single or continuous conversion mode.
7. Separate 10-bit result register for each input channel.

4.2 Application description

4.2.1 Design rules

No advisable restrictions.

4.2.2 Application diagram

Fig 3 shows how the 10-bit ADC should be connected when used and when not used. If not used then the supply pin (pin V10) must be tied to ground which prevents floating inputs internally. The Analog inputs can be left open.

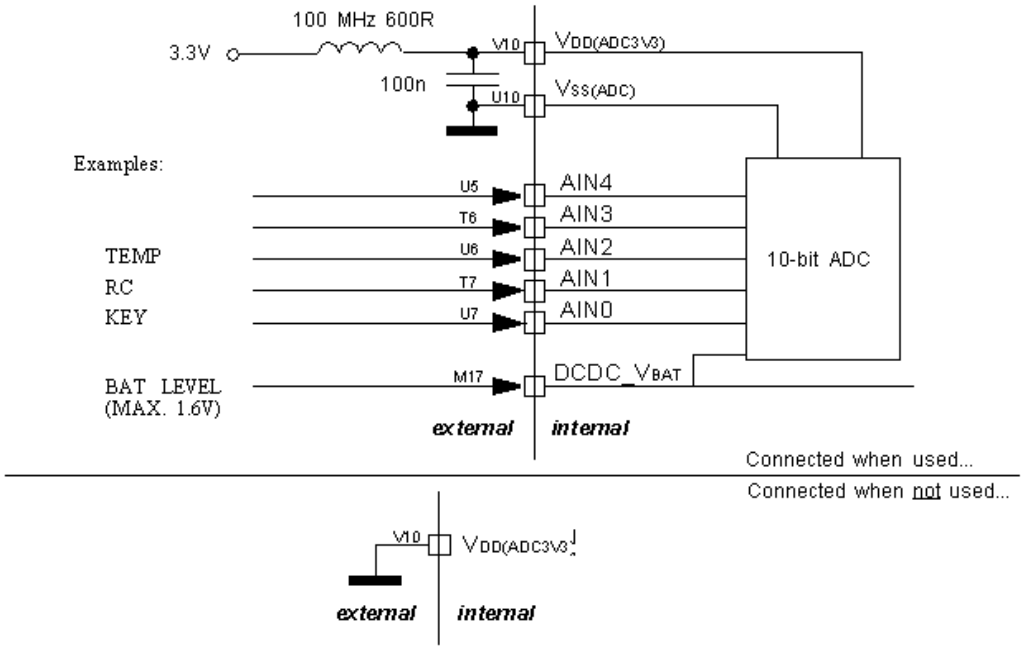


Fig 3. 10-bit ADC connection

5. LCD interface

5.1 Overview

1. 4-bit or 8-bit external data bus, or serial data, for connection to LCD or other devices.
2. 8080 or 6800-compatible parallel mode.
3. Software-configurable control signals for glue-logic-free connection.
4. 16-byte output FIFO.
5. Optional hardware polling of busy/ready status.
6. Flow control for use with GPDMA channel.

5.2 Application description

5.2.1 Design rules

No advisable restrictions

5.2.2 Application diagram (8-bit parallel mode)

Fig 4 shows how the LCD interface should be connected when used in 8-bit parallel mode. When the LCD interface is not used all pins can be left unconnected. In software this module should be set in power down mode and all pins as outputs.

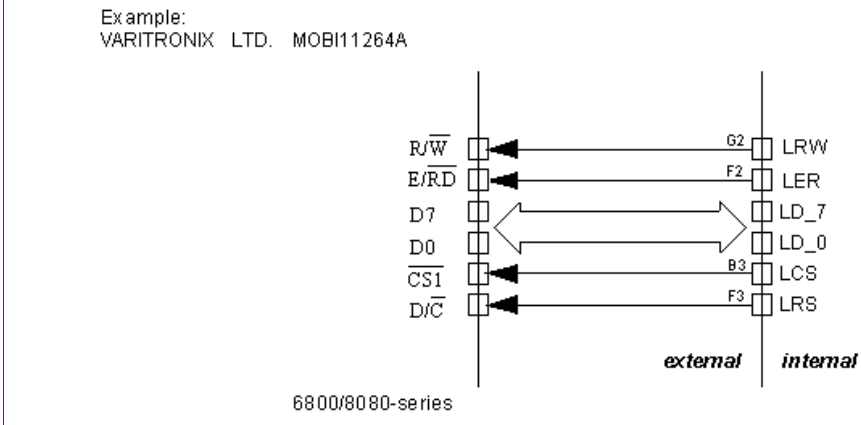


Fig 4. LCD interface connection (8-bit parallel mode)

5.2.3 Application schematic (4-bit parallel mode)

Fig 5 shows how the LCD interface should be connected when used in 4-bit parallel mode.

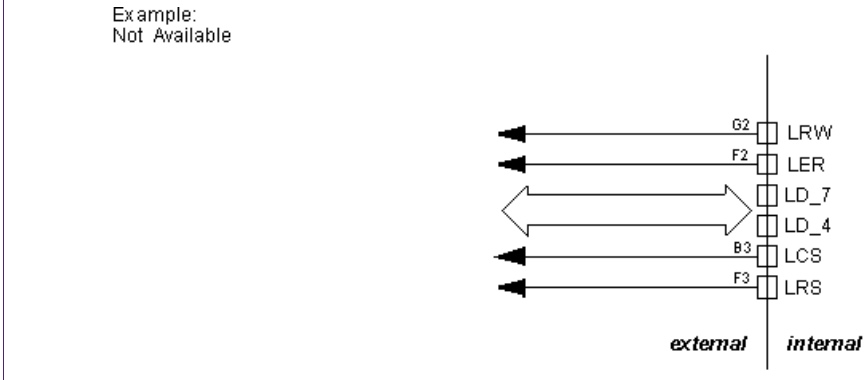


Fig 5. LCD interface connection (4-bit parallel mode)

5.2.4 Application schematic (serial mode)

Fig 6 shows how the LCD interface should be connected when used in serial mode.

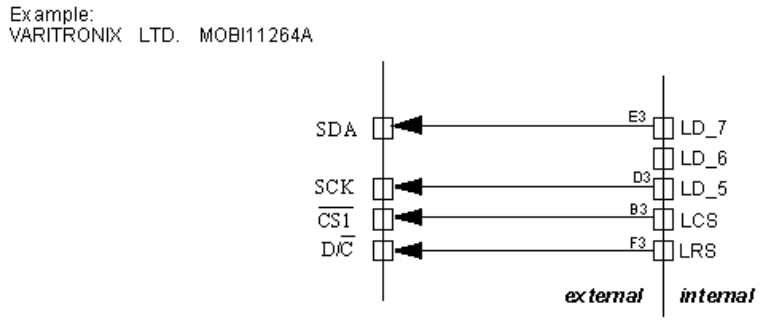


Fig 6. LCD interface connection (serial mode)

6. SD/MMI interface

6.1 Overview

The Secure Digital and Multimedia Card Interface (SD/MCI) is an interface between the Advanced Peripheral Bus (APB) system bus and multimedia and/or secure digital memory cards. It consists of two parts:

1. The MCI adapter block provides all functions specific to the Secure Digital/Multimedia memory card, such as the clock generation unit, power management control, command and data transfer.
2. The APB interface accesses the SD/MCI registers, and generates interrupt and DMA request signals.

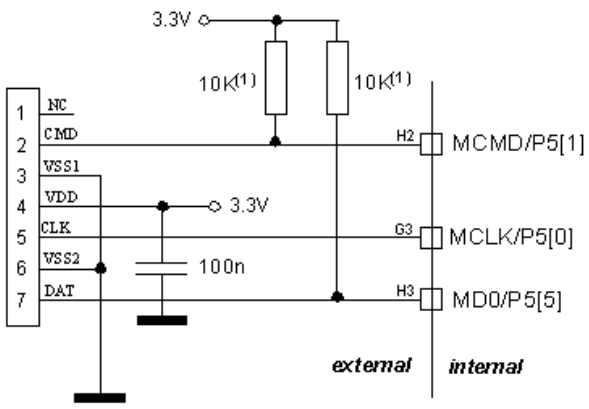
6.2 Application description

6.2.1 Design rules

The value of the pull up resistors is not fixed.

6.2.2 Application schematic (Multi Media Card)

Fig 7 shows how the MCI should be connected when used as a MultiMediaCard (MMC) Interface. When the MCI is not used all pins can be left unconnected. In software this part should then be set to Power-down mode and all pins as outputs.



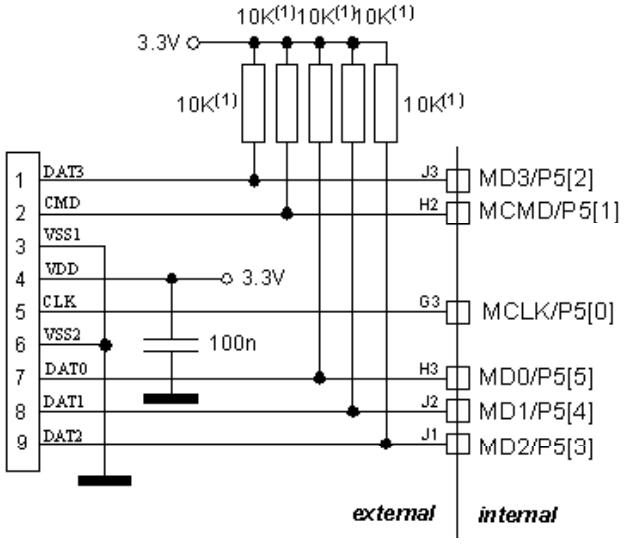
(1) The pull-up resistor value is not fixed.

Fig 7. MCI connection when used as an MMC interface

6.2.3 Application diagram (Secure Digital)

Fig 8 shows how the MCI should be connected when used as a Secure Digital Card Interface.

When the MCI is not used all pins can be left unconnected. In software this part should then be set to power down mode and all pins as outputs.



(1) The pull-up resistor value is not fixed.

Fig 8. MCI connection when used as an SD card interface

7. USB Interface

7.1 Overview

The USB Interface of the LPC288x is a High Speed USB Interface (480 Mbit/s), which also supports Full Speed and is USB 2.0 compliant.

7.2 Application description

7.2.1 Design rules

For the High Speed Interface to function correctly, correct layout is essential. PCB layout guidelines can be found at the end of this chapter.

7.2.2 Application diagram

Fig 9 shows how the USB Interface should be connected when used as a High Speed USB Interface (480 Mbit/s).

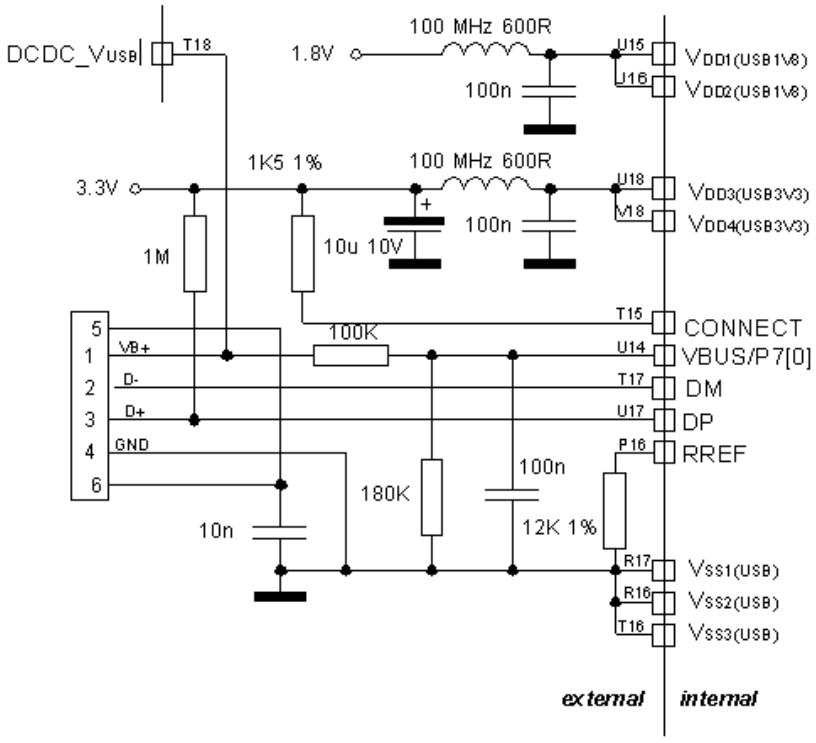


Fig 9. USB interface connection (High speed USB interface)

7.2.3 PCB layout guidelines

For High Speed signals the traces on the PCB, should ideally only run on one layer, the top layer and not pass through structures (i.e. vias), which can cause impedance mismatches. The traces should be impedance matched to 45 Ω and should be as short as possible and preferably not have any 90 degree angles: curves will minimise reflections. In some cases this might not be possible, but on the PCB great care should be taken with these traces and with the return ground to $V_{SS3(USB)}$

As far as the analog and digital ground planes are concerned, the normal practice is to separate these planes and run the analog plane over the analog sections (DP/DM traces only) and the digital plane over the digital sections.

8. JTAG

8.1 Overview

The LPC288x has a JTAG Interface, which can be used to connect the internal ARM7TDMI-S core to the ARM Multi-ICE™ or any other JTAG emulator for software development and debugging.

8.2 Application description

8.2.1 Design rules

No advisable restrictions.

8.2.2 Application diagram

Fig 10 shows how the JTAG Interface should be connected when used with any standard JTAG emulator.

The connection between pin 1 of the JTAG connector and $V_{DD1(IO3V3)}$ to $V_{DD6(IO3V3)}$ needs to be provided to ensure that the level of the external pads of the LPC288x is the same as that of the JTAG emulator.

If the JTAG Interface is not used all pins can be left unconnected. Internal pull down/up resistors determine all levels of the JTAG pins.

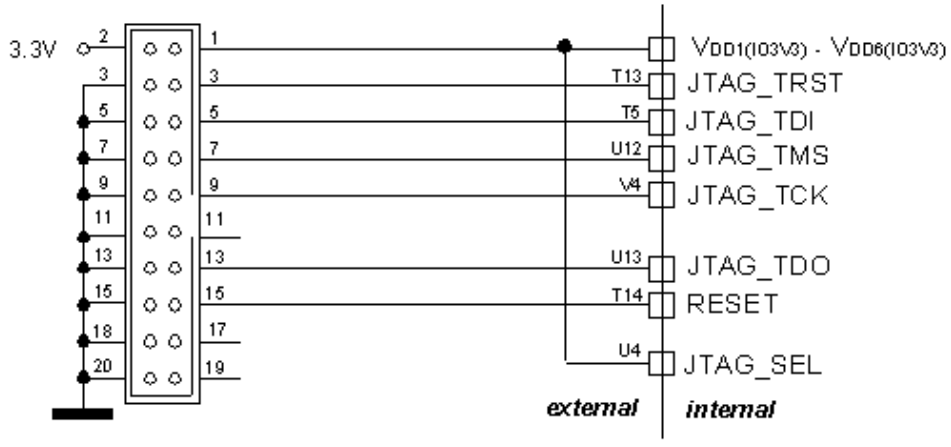


Fig 10. JTAG interface connection with JTAG emulator

9. I²C master/slave interface

9.1 Overview

1. Standard I²C bus interface, configurable as Master, Slave, or Master/Slave.
2. Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.

3. Programmable clock allows adjustment of I²C transfer rates.
4. Bidirectional data transfer between masters and slaves.
5. Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
6. Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
7. Supports normal (100 kHz) and fast (400 kHz) operation.

9.2 Application description

9.2.1 Design rules

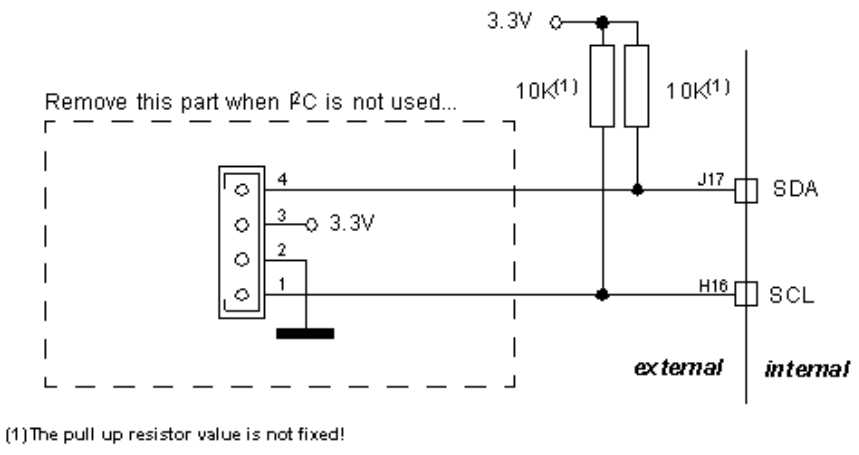
The value of the pull up resistors is not fixed, meaning that depending of the application, which can be using the I²C in normal or fast mode this resistor value needs to be changed to meet the I²C signal specification. Also the load and layout of the I²C lines in the application can play a role in determining the resistor value.

9.2.2 Application diagram

Fig 11 shows how the I²C Master/Slave Interface should be connected when used.

When the I²C Master/Slave Interface is not used the pull up resistors are still needed, the rest of the components can be removed.

For further details please refer to the I²C-bus specification.



(1) The pull-up resistor value is not fixed.

Fig 11. Connection of the I²C master/slave interface

10. External memory controller

10.1 Overview

The LPC288x External Memory Controller (EMC) is a multi-port memory controller that supports asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as Single Data Rate SDRAM. It complies with ARM's Advanced Microcontroller Bus Architecture (AMBA).

10.2 Application description

10.2.1 Design rules

No advisable restrictions.

10.2.2 Application diagram (SDRAM)

Fig 12 shows how the EMC interface should be connected when used with a 64 Mbit SDRAM.

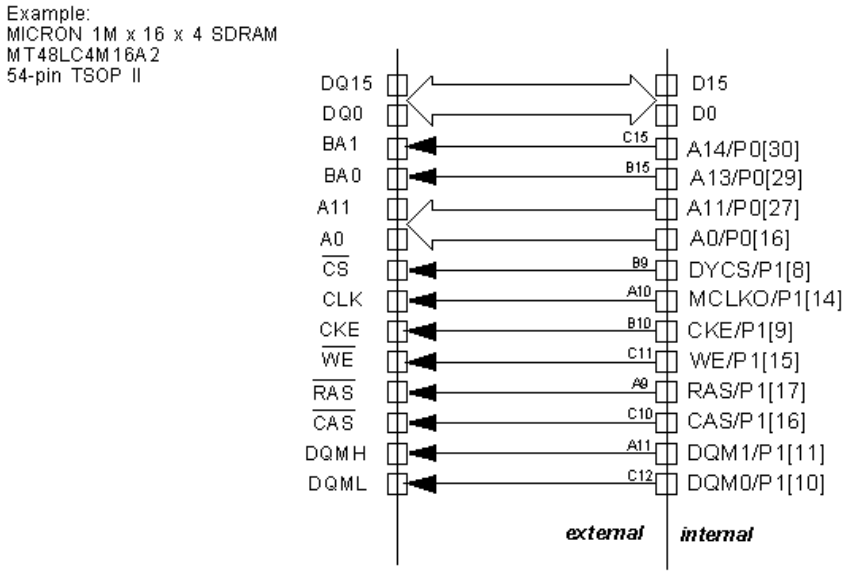


Fig 12. EMC interface connection with 64 Mbit SDRAM

10.2.3 Application diagram (SyncFlash)

Fig 13 shows how the EMC Interface should be connected when used with a 64 Mbit SyncFlash.

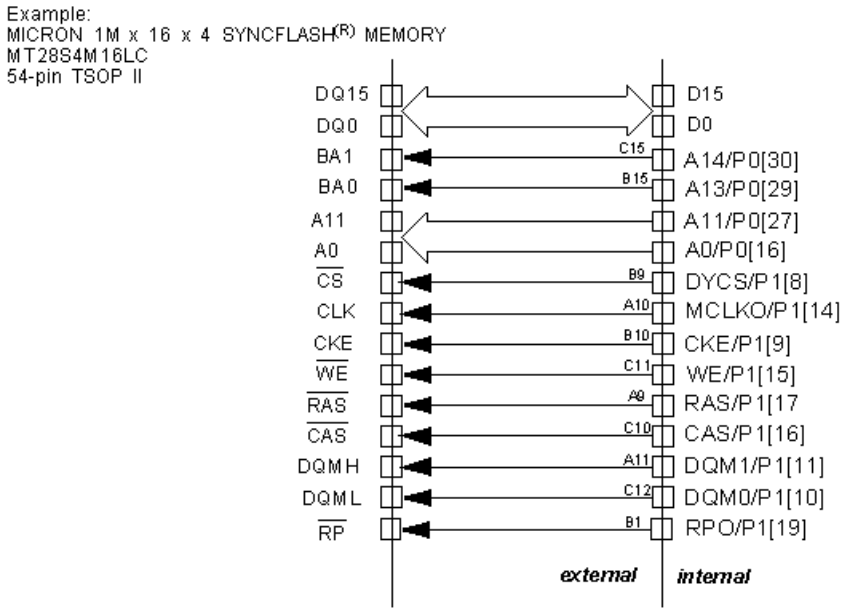


Fig 13. EMC interface connection with 64 Mbit SyncFlash

10.3 Application diagram (SRAM)

Fig 14 shows how the EMC should be connected when used with SRAM.

The given example is based on a 16-bit wide SRAM, where A0 is not the byte/word select. When using another 16-bit wide memory device were A0 is used as byte/word select, A0 should be connected to A1 instead of A0.

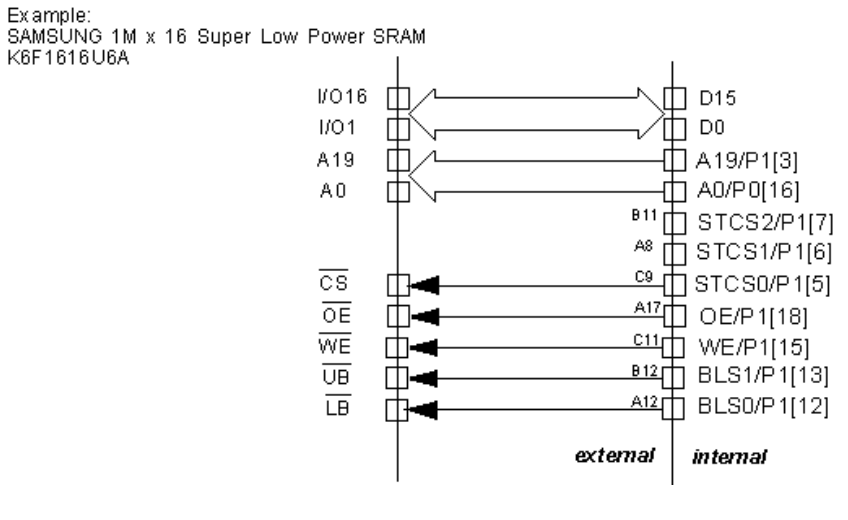


Fig 14. EMC interface connection with 16-bit wide SRAM

10.3.1 Application diagram (NOR flash)

Fig 15 shows how the EMC should be connected when used with NOR flash.

The example given is specific for this device, maybe it is applicable to more devices, but this has not been checked.

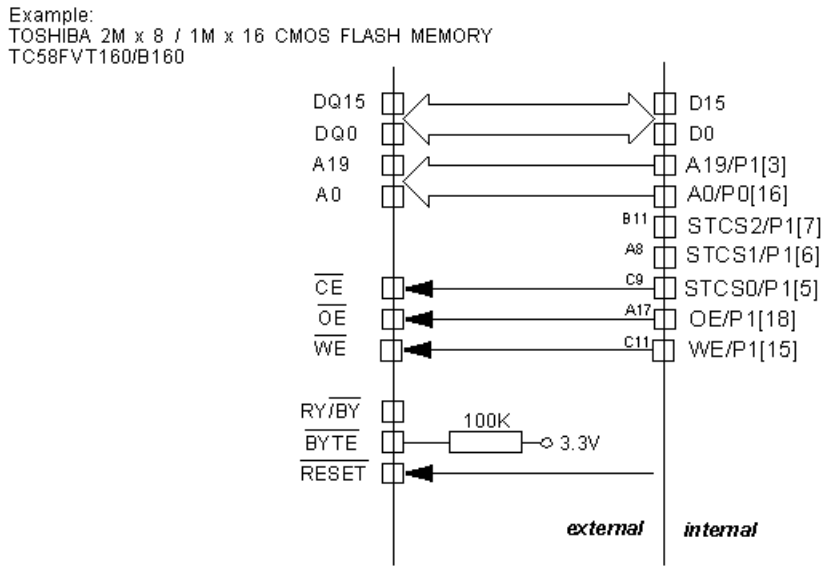


Fig 15. EMC interface connection with NOR flash

11. UART

11.1 Overview

1. 32 byte Receive and Transmit FIFOs.
2. Superset of the ’650 industry standard.
3. Receiver FIFO trigger points at 1, 16, 24, and 28 bytes.
4. Built-in baud rate generator.
5. CGU generates UART clock including fractional divider capability.
6. Autobaud capability.
7. CTS input and RTS output, with optional hardware flow control.
8. IrDA mode for infrared communication.

11.2 Application description

11.2.1 Design rules

No advisable restrictions.

11.2.2 Application diagram

Fig 16 shows how the UART should be connected when used.

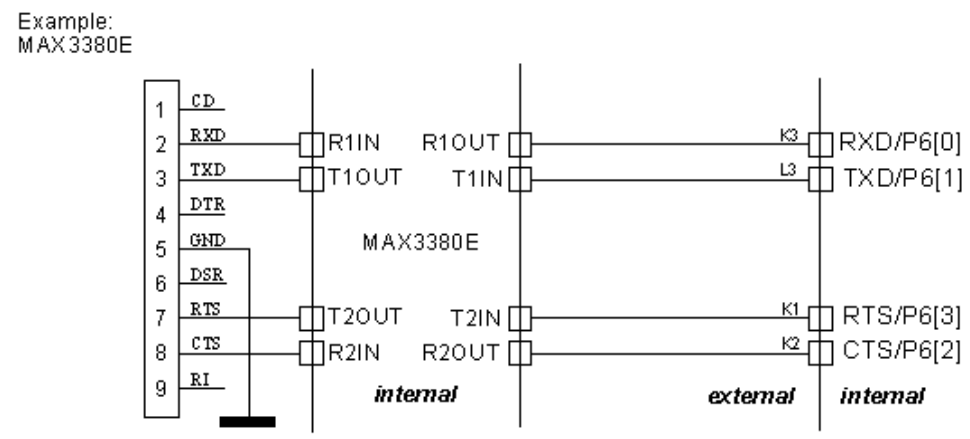


Fig 16. Connection of UART

Fig 17 shows how the UART should be connected when used as Infrared communication.

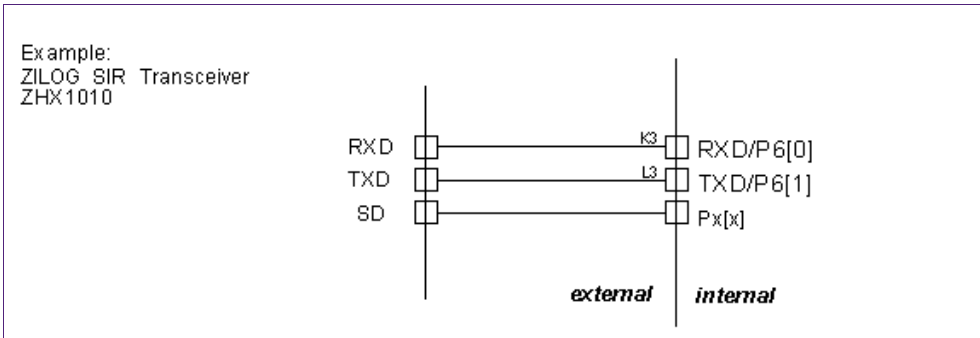


Fig 17. Connection of UART when used as IR communication

12. IO configuration and pinning

12.1 Overview

1. TFBGA180 package: Plastic low-profile ball grid array, 180 balls, 10 x 10 x 0.8 mm.
2. 81 pins have dual use General Purpose I/O or “functional” I/O, plus 4 dedicated GPIO.
3. Each dual use pin can be programmed for functional I/O, drive high, drive low, or hi-Z/input.
4. 4 pins dedicated General Purpose I/O, programmable for drive high, drive low, or hi-Z/input.

12.2 Application description

12.2.1 Design rules

When using the Mode Selection pins as GPIO pins in the design take care of the fact that it is designed in that way that during start up the correct mode is selected.

12.2.2 Application schematic

Fig 18 shows how the Mode Selection pins should be connected when used.

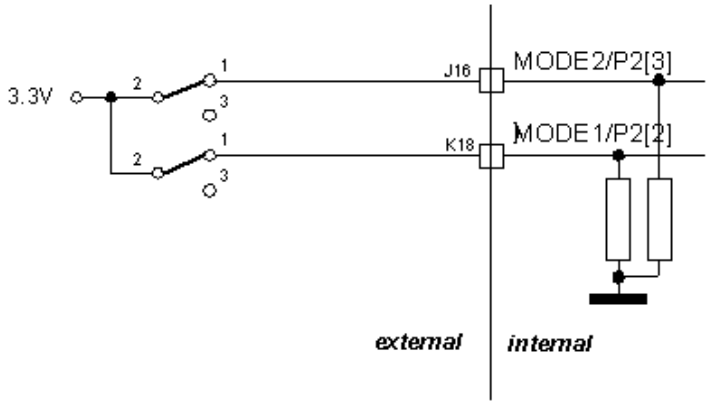


Fig 18. Connecting mode selection pins

13. Digital supplies

13.1 Overview

The following are referred as digital supplies:

1. $V_{DD1(CORE1V8)}$, $V_{DD2(CORE1V8)}$, $V_{DD2(FLASH1V8)}$, $V_{DD1(FLASH1V8)}$
2. $V_{SS1(CORE)}$, $V_{SS2(CORE)}$, $V_{SS3(CORE)}$

13.2 Application description

13.2.1 Design rules

Decoupling of the digital supplies is done internally and should be sufficient so that for these supplies no external decoupling is needed.

13.2.2 Application schematic

Fig 19 shows how the digital supplies can be connected to an external supply.

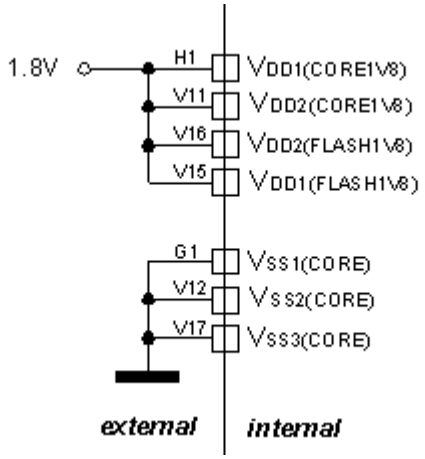


Fig 19. Connecting digital supplies to an external supply

14. Peripheral supplies

14.1 Overview

The following supplies are referred to as peripheral supplies:

1. $V_{DD1(IO3V3)}$, $V_{DD2(IO3V3)}$, $V_{DD3(IO3V3)}$, $V_{DD4(IO3V3)}$, $V_{DD5(IO3V3)}$, $V_{DD6(IO3V3)}$
2. $V_{DD1(EMC)}$, $V_{DD2(EMC)}$
3. $V_{SS1(IO)}$, $V_{SS2(IO)}$, $V_{SS3(IO)}$, $V_{SS4(IO)}$, $V_{SS5(IO)}$, $V_{SS6(IO)}$
4. $V_{SS1(EMC)}$, $V_{SS2(EMC)}$

14.2 Application description

14.2.1 Design rules

Decoupling of the peripheral supplies needs to be done externally.

14.2.2 Application diagram

Fig 20 shows how the peripheral supplies can be connected to an external supply. $V_{DD5(IO3V3)}$, $V_{DD6(IO3V3)}$ though not shown below will have similar connections as the other $V_{DDX(IO3V3)}$. Similarly, $V_{SS5(IO)}$, $V_{SS6(IO)}$ will have follow $V_{SSX(IO)}$.

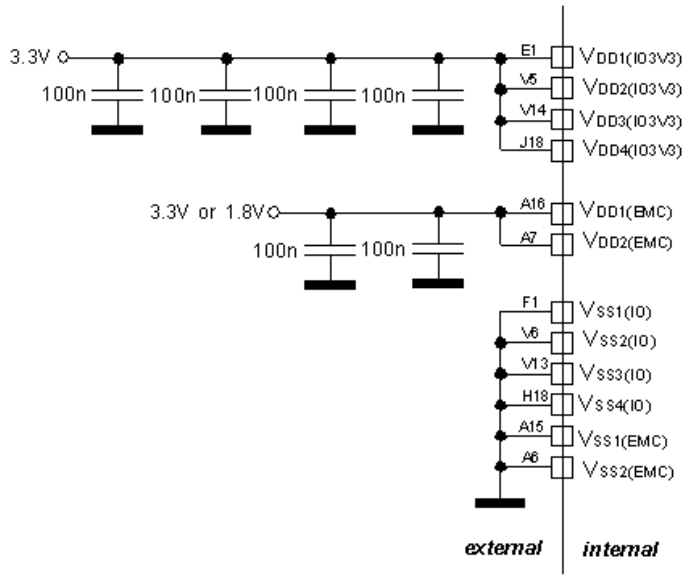


Fig 20. Connecting peripheral supplies to an external supply

15. I²S input module (DAI) and I²S output module (DAO)

15.1 Overview

The LPC288x can input a single- or dual-channel audio stream from an Inter-IC Sound (I²S) bus. The I²S input module is called the DAI. It can capture serial data in standard Philips IIS format, or in right-justified 16-, 18-, 20-, or 24-bit format.

The LPC288x can output a single- or dual-channel audio stream to an I²S bus. The I²S output module is called the DAO. It can output serial data in standard Philips IIS format, or in right-justified 16-, 18-, 20-, or 24-bit format.

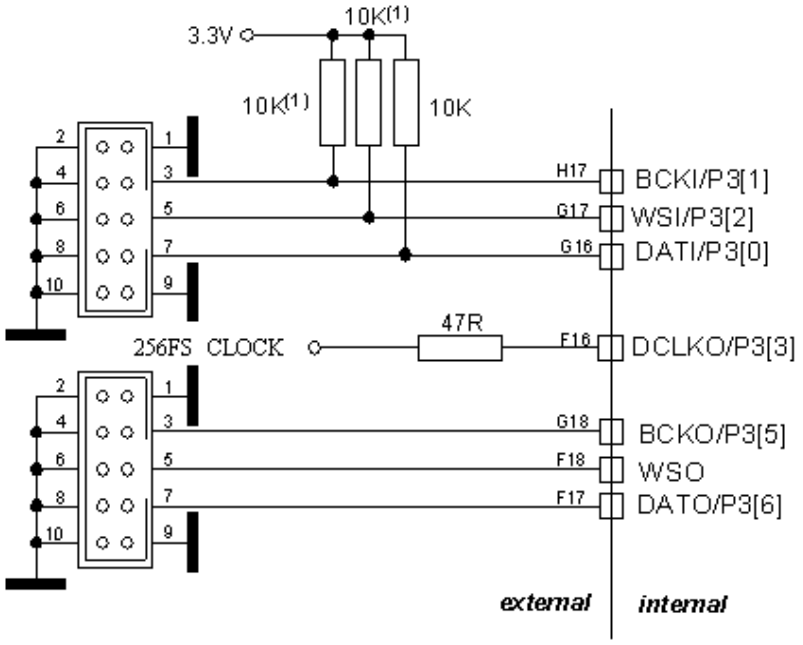
15.2 Application description

15.2.1 Design rules

The BCK and WS can also be used in I²S master mode, meaning that these inputs can also be switched as outputs to generate a bit clock and word select for a slave device. In this case the slave only returns the data.

15.2.2 Application diagram

Fig 21 shows how the DAI and DAO Interface should be connected when used.



(1) When BCKI and WSI are in I2S master mode, these pull-ups are not needed.

Fig 21. Connecting DAI and DAO interface

16. Dual channel 16-bit analog to digital converter

16.1 Overview

The ADC circuitry consists of two identical 16-bit Sigma-Delta converters. In order to allow use for synchronized sampling applications, such as I-V measurements for power factor calculations or stereo audio, the converters are synchronized so that the two channels operate on “left” and “right” data, which are sampled at the same time.

16.2 Application description

16.3 Design rules

AINR and AINL both need to be foreseen with a 1 MΩ pull-down resistor to ground. Both resistors need to be as close as possible to the inputs of the IC for the suppression of idle tones.

16.4 Application diagram

Fig 22 shows how the ADC should be connected when used. When this part is not used the supplies must be connected and the inputs can be left open. In software this part must be set in power down using the power control registers in the CGU (Clock Generation Unit).

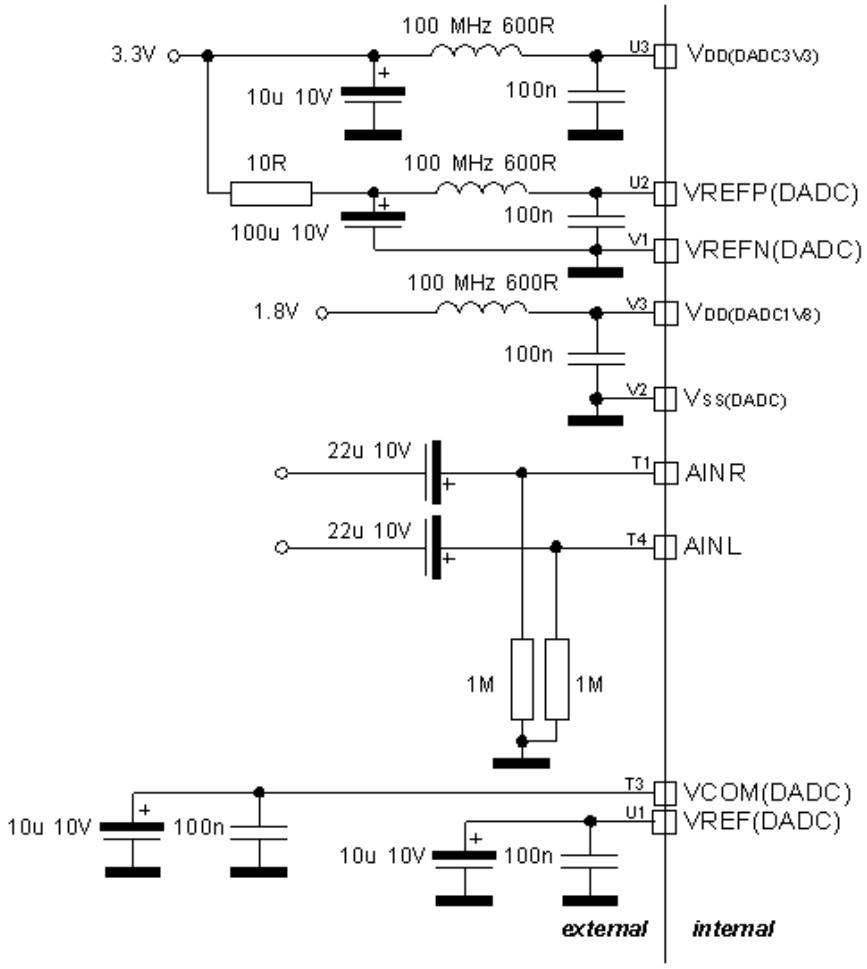


Fig 22. Connecting ADC

17. Dual channel 16-bit digital to analog converter

17.1 Overview

The dual channel bitstream DAC can be used for stereo audio and other one- or two-channel D-to-A applications, particularly those involving regular, periodic conversion. The basic architecture of the block consists of an input block that receives 24-bit inputs at the Nyquist sample frequency of interest (fs), up-samples and interpolates to 128 fs using 16-bit coefficients and performs noise shaping, after which the digital results are converted to analog voltages.

17.2 Application description

17.2.1 Design rules

Because of the low rejection ratio of VREFP and VREFN the supply to these pins needs to be very clean to prevent unwanted distortion in the audio signal. One of the possibilities to do this is to provide a big capacitor between VREFP and VREFN. If even

higher audio performance is needed then it is advised to provide an external LDO which is going to provide the supply for the SDAC.

17.2.2 Application diagram

Fig 23 shows how the DAC should be connected when used. The schematic shows how to connect the DAC with VREFP decoupling. The schematic also shows how to connect the DAC with an external LDO.

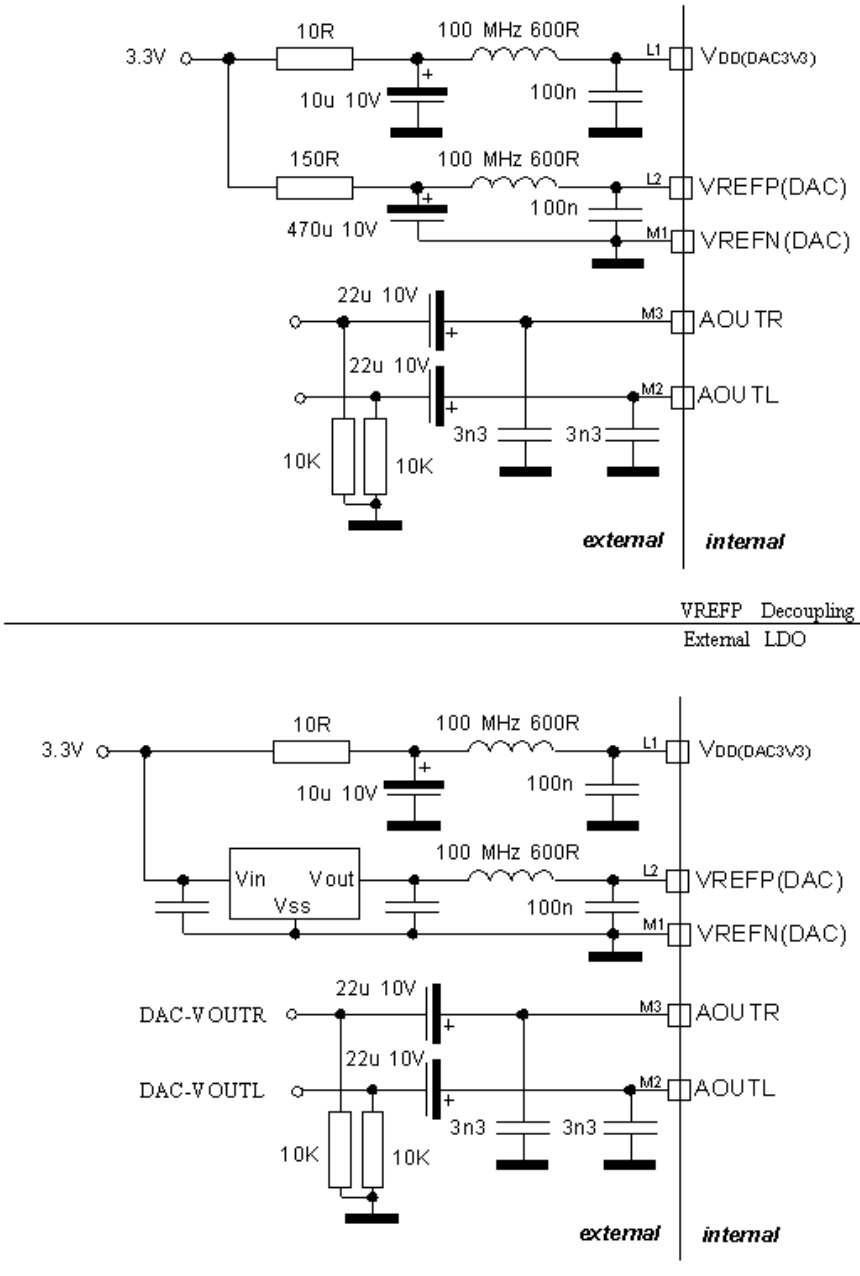


Fig 23. Connecting DAC

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